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Silicon integrated circuit thermoelectric generators with a high specific power generation capacity

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Microelectronic thermoelectric generators (TEGs), which can recycle waste heat into electrical power, have applications ranging from the on-chip thermal management of integrated circuits to environmental energy sources for Internet-of-things sensors. However, the incompatibility of TEGs with silicon integrated circuit technology has prevented their broad adoption in microelectronics. Here, we report TEGs created using nanostructured silicon thermopiles fabricated on an industrial silicon complementary metal–oxide–semiconductor (CMOS) process line. These TEGs exhibit a high specific power generation capacity (up to 29 μW cm^{-2} K^{-2}) near room temperature, which is competitive with typical $(Bi,Sb)_2(Se,Te)_3$-based TEGs. The high power capacity results from the ability of CMOS processing to fabricate a very high areal density of thermocouples with low packing fraction and to carefully control electrical and thermal impedances. TEG power was also found to increase significantly when thermocouple width was decreased, providing a path to further improvements. Unlike $(Bi,Sb)_2(Se,Te)_3$ TEGs, our silicon integrated circuit TEGs could be seamlessly integrated into large-scale silicon CMOS microelectronic circuits at very low marginal cost.

Thermoelectric generators (TEGs) are attractive as an environmentally clean technology for converting waste heat into electrical power. Bulk TEGs are used to generate power from heat sources[1] such as vehicle engines, power plants and solar concentrators[2]. Recently, microelectronic thermoelectric (TE) devices aimed at integrated circuit (IC) and sensor applications such as on-chip thermal management[3,4], biothermal power for wearable electronics[5,6] and near-room-temperature waste heat harvesting[7,8] have been explored. Microelectronic TEGs are of potential value in the Internet-of-things (IoT), which will comprise a network of low-power microsensors embedded into a variety of environments. For IoT sensors, microelectronic TEGs could provide a long-term power source in situations where regular access for battery replacement is impractical or insufficient light exists for photovoltaics, but a reliable thermal gradient exists[9,10].

Current research on TEGs typically focuses on materials that have a high TE figure-of-merit ZT; $ZT=(S^2/\rho\kappa)T$, where S is the Seebeck coefficient, ρ is the electrical resistivity, κ is the thermal conductivity and $T=\frac{1}{2}(T_H+T_C)$, where T_H is the hot and T_C the cold temperature (in K) across the TEG. High-ZT materials are valued because the efficiency η increases with ZT (refs. [11,12]; $\eta=P/Q_H$, where P is the power generated and Q_H is the heat inflow from T_H). Widely researched high-ZT materials such as the $(Bi,Sb)_2(Te,Se)_3$ system or PbTe have $ZT\approx1$ near room temperature[9]. Half-Heusler alloys[13] and skutterudites[14] have $ZT\approx1$ at ≥500 °C. However, use of these materials in microelectronics is restricted because they are incompatible with industrial Si complementary metal–oxide–semiconductor (CMOS), by far the dominant microelectronic technology, making it difficult to incorporate high-ZT TEGs into Si integrated circuits. Post-processing offers a possible route[3] but at high marginal cost, which limits commercial acceptance.

Historically, Si has not been considered for TE applications because bulk silicon has a ZT of ~10^{-3} to 10^{-2} near room temperature[15]. This began to change in 2008 when it was reported[16,17] that Si nanowires can have ZT values up to 0.6, making Si potentially competitive with high-ZT materials. This ZT increase has been attributed to the suppression of phonon thermal conduction by scattering from the Si surface. Surface suppression of phonon heat transport should be important when the cross-sectional dimensions for heat flow become smaller than the phonon mean free path, 50–200 nm in Si (ref. [18]). This explanation is supported by empirical observations[16] and by numerical simulations and theory[19–22].

These findings have prompted numerous efforts to develop microelectronic TEGs with Si nanowires[10,22–27] or other micro- or nanostructured Si thermopiles[28–31]. However, the thermopile characteristics and efficiencies reported for these nanostructured Si TEGs, which were fabricated using photolithographic mask and etch techniques, are consistent with $ZT\leq\sim10^{-2}$, significantly smaller than reported in refs. [16,17]. Consequently, the efficiency of Si TEGs has lagged behind that of high-ZT materials.

In practice, efficiency is not necessarily the primary concern in many applications, but rather how much power a TEG of given size generates from a temperature difference $\Delta T=T_H-T_C$ and cost per watt[32]. Because the maximum power P_{max} generated is proportional both to $(\Delta T)^2$ and to cross-sectional area A for heat flow[11], a performance metric of more direct practical interest is the specific power generation capacity $\Gamma_P=P_{max}/[A(\Delta T)^2]$, as this measures the TEG output power scaled to the device size and to ΔT. (Ref. [33] calls Γ_P the TE efficiency factor.) Γ_P is an extrinsic device metric that can be engineered by circuit design and the management of parasitic impedances[34].

The best Γ_P values compiled from tabulated summaries[7,24,33] of $(Bi,Sb)_2(Te,Se)_3$ TEGs range from 2 to 150 μW cm^{-2} K^{-2}, usually in harvest mode, which uses an external hot reservoir and so includes an external contact thermal impedance. Harvest mode results are meaningful application benchmarks but can vary depending on exact test conditions[35]. The test mode, where an integrated heater avoids the external contact impedance and so typically gives higher power than the harvest mode, may better demonstrate the intrinsic capabilities of a TEG. The highest reported[10] Γ_P for a Si TEG is 0.48 μW cm^{-2} K^{-2} (harvest mode). (Ref. [22] reports results implying Γ_P of 373 μW cm^{-2} K^{-2} (test mode), but their fig. 8 shows that

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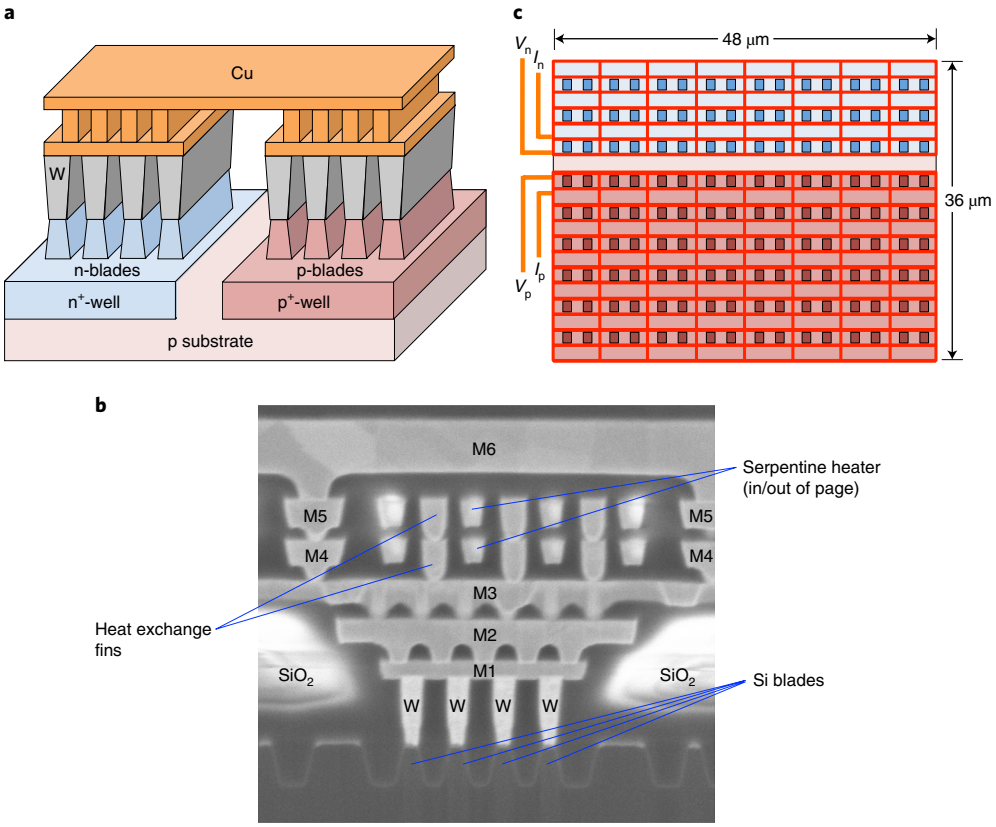

Fig. 1 | Description of TEG devices. a, Block sketch (not to scale) of a thermocouple pair consisting of a group of four n-type and a group of four p-type nanoblades contacted by W plugs. **b**, SEM cross-section of a single four-blade group with W contacts, metal heat exchange/conduction metal layers and a serpentine heater. The top of each blade is 80 nm wide. **c**, Plan view sketch of a thermopile layer, without the metal layers. Groups of n-blades are designated as darker blue rectangles and groups of p-blades as darker red rectangles. The bright red grid is a silicide contact matrix, connected to external voltage (V_n, V_p) and current (I_n, I_p) leads.

much of the power is not generated by their nanowire arrays and does not scale with area.) More commonly[23–31], Si-based TEGs have Γ_P values between 0.01 and 0.04 μW cm^{-2} K^{-2} in either harvest or test mode. Thus, a reasonable threshold for Si TEGs to be competitive with $(Bi,Sb)_2(Te,Se)_3$ is to demonstrate a Γ_P of 1–10 μW cm^{-2} K^{-2} in harvest mode or 10–100 μW cm^{-2} K^{-2} in test mode, while retaining the scalability, integration and cost advantage benefits of CMOS technology

A critical requirement for TEGs to gain broad acceptance is the ability to assimilate TEG circuits into commercial CMOS processing. While advances[10,22–31] in Si TEGs thus far have used CMOS-compatible fabrication methods, these works did not explicitly comply with the strict design rules of industrial Si CMOS processing that ensure compatibility of all circuits on a chip. In this Article, we report on Si IC TEGs fabricated on a standard 65 nm technology node CMOS process line with no additional mask or process steps. Consequently, these IC TEGs can be seamlessly integrated into large-scale IC technology without increasing the cost or complexity.

Si nanoblade IC TEG device design

The details and dimensions of the Si IC TEG fabrication are provided in the Methods. The thermopile elements are doped Si nanostructured blades having a mask-defined width, though not length, less than or equal to the phonon mean free path. Although nanowire geometries may give higher ZT values, a blade geometry is used here to comply with standard process design rules. Figure 1a illustrates (not to scale) a simplified thermopile structure with a thermocouple formed by a pair of four-blade groups. The blade tops are contacted by tungsten plugs. Metal layers connect all n-groups in parallel and, separately, all p-groups in parallel. Higher metal layers connect the n- and p-sides to form thermocouples. Figure 1b shows a scanning electron microscope (SEM) image of a cross-section through one four-blade group. Near the top, a resistive heater consisting of a thin serpentine Cu line (winding in and out of the page) is used as both heater and thermometer, so all measurements are in test mode. This heater is surrounded by a Cu box formed by metal layers M3–M6 connected by vias, with heat exchange fins between the heater lines. This box transfers heat to metal layers M1 and M2 at the top of the thermopile with the goal of minimizing parasitic series thermal impedance. Large regions of the SiO_2 filler appear white because of charging effects.

Figure 1c presents a plan view illustration of the thermopile layer in a baseline TEG. In operation, heat flows into the plane of the page. The blue-shaded portion represents the n$^+$-well. The reddish-shaded portion represents the p$^+$-well. The n- and p-blade groups, represented by darker blue (n-blades) and darker red (p-blades) rectangles, are laid out in a rectangular array. The blade groups are surrounded by a highly electrically conducting silicide grid, drawn as thicker bright red lines, contacting the n$^+$- and p$^+$-wells. The silicide grid is contacted by metal leads to form a Kelvin probe configuration. More p-blades were used to balance the electrical resistance between the n- and p-sides because p-type Si has a higher resistivity at a similar dopant density. Packing fraction, the ratio of the cross-sectional area of all thermopile blades to total device area, is ~2%.

To explore the effect of circuit layout and design on TEG performance, many variations in TEG design were fabricated. Variations included different nanoblade groupings, widths, electrical contact areas and metal layering structures to conduct heat to the thermopile.

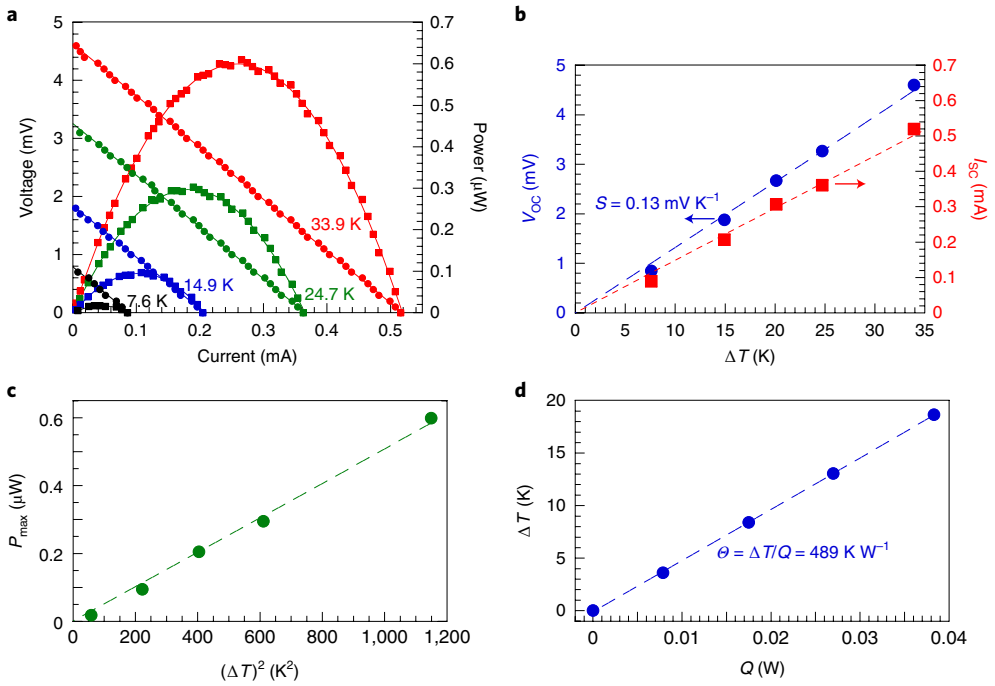

Fig. 2 | Performance data on a TEG. a, Voltage (circles) and power (squares) versus current at applied temperature differences (ΔT) of 7.6, 14.9, 24.7 and 33.9 K from the TEG with the highest Γ_P. Solid lines are least-squares linear (for voltage) or quadratic (for power) fits. **b**, Open-circuit voltage V_{OC} and short-circuit current I_{SC} versus ΔT for the same DUT as in **a**. Dashed lines are least-squares linear fits. The slope $S = \Delta V_{OC}/\Delta T = 0.13\,\text{mV K}^{-1}$ gives the net thermopower. **c**, Maximum power $P_{max} = \frac{1}{4} V_{OC} I_{SC}$ versus $(\Delta T)^2$. The dashed line is a least-squares linear fit. **d**, ΔT plotted versus applied heater power $Q = V_{heat} I_{heat}$. The slope of the dashed line least-squares linear fit gives the total thermal impedance, Θ.

The different TEG circuit variants helped to correlate performance with nanoblade dimensions and sources of parasitic electrical and thermal impedances. In total we measured over 300 individual devices under test (DUTs), representing 19 TEG circuit variations.

Measurement results

Measurement details are described in the Methods. Shown here are data from one DUT with the circuit layout giving the highest Γ_P in test mode. The circuit design for this DUT used the baseline blade dimension with three four-blade groups per silicide cell, rather than the two groups per cell shown in Fig. 1c, but had the baseline planar area $A = 48\,\mu\text{m} \times 36\,\mu\text{m}$. Data for all circuit variant types showed the same functional characteristics, but with type-specific values of performance parameters.

Figure 2a shows a family of thermopile current–voltage (I–V) data at several ΔT, plotted with TE power $P = VI$. For clarity, not all values of ΔT measured are shown. The I–V plots are linear with constant slope; increasing ΔT offsets the I–V line away from the origin. The slope $R_S = |\Delta V/\Delta I| = 9\,\Omega$ is the source resistance. All DUTs of the same circuit type on the same die had the same R_S to within 5%. Across DUTs of different circuit types, R_S ranged from ~10 to 70 Ω, with most between 22 and 28 Ω. At fixed ΔT, the open-circuit voltage V_{OC} and the short-circuit current I_{SC} are the I–V intercepts with the voltage and the current axes. Because I–V is linear, P is a quadratic function of I with maximum $P_{max} = \frac{1}{4} V_{OC} I_{SC} = (V_{OC})^2/4R_S$. P_{max} corresponds to the power generated when R_S = load resistance R_L (matched load).

Figure 2b shows that both V_{OC} and I_{SC}, taken from Fig. 2a, are proportional to ΔT. The slope $\Delta V_{OC}/\Delta T = 0.13\,\text{mV K}^{-1}$ gives the net Seebeck coefficient $S = S_n - S_p$, including parasitic impedances. Because there are no electrical taps between the n- and p-sides, S_n and S_p cannot be measured separately. Figure 2c shows $P_{max} \propto (\Delta T)^2$, as expected, with slope $P_{max}/(\Delta T)^2 = 5.1 \times 10^{-4}\,\mu\text{W K}^{-2}$. This gives $\Gamma_P = P_{max}/[A(\Delta T)^2] = 29\,\mu\text{W cm}^{-2}\text{K}^{-2}$. Among all the TEG variants with 80 nm blade width, Γ_P ranged from 1.5 to 29 $\mu\text{W cm}^{-2}\text{K}^{-2}$, with mode and median of 8.5 $\mu\text{W cm}^{-2}\text{K}^{-2}$.

Thermal impedance was determined using the 'hot strip' method.[36] The measured thermal impedance $\Theta_{meas} = \Delta T/Q$, where $Q = V_{heat} I_{heat}$, is the heat flow under open-circuit conditions, known from the temperature controller's bias outputs. Figure 2d shows that ΔT is linearly related to Q with slope $\Theta_{meas} = 489\,\text{K W}^{-1}$, including parasitic series and leakage thermal impedances. DUTs of the same circuit type had the same Θ_{meas} to within 5%. Across different circuit types, Θ_{meas} ranged from 300 to 1,200 K W^{-1}, with most types having Θ_{meas} between 500 and 600 K W^{-1}.

Electrical and thermal impedance modelling

To understand the relationship between circuit type variations, empirical characteristics like R_S and Θ_{meas} and performance metrics such as Γ_P, we developed a detailed model of the electrical and thermal impedances. Details of the modelling procedure are provided in the Methods.

Figure 3a presents a scatter plot of modelled electrical resistance R_{model} versus measured R_S across 19 circuit variations (with the same dopant densities) along with the least-squares fit line. Each point represents a DUT of one circuit variant with its particular layout geometry and dimensions used to calculate R_{model}, but every point in Fig. 3a uses the same material resistivity values determined from the least-squares fit. If R_{model} exactly described R_S, the plot would be linear with unity slope. Figure 3a shows that R_{model} is linearly related to R_S with a slope of 0.973 and coefficient of determination $r^2 = 0.991$. This indicates that the model provides a very good physics-based representation of the internal electrical resistances.

This model helps isolate the intrinsic thermopile resistance R_{TP} and gives clear guidance about how geometric and dimensional

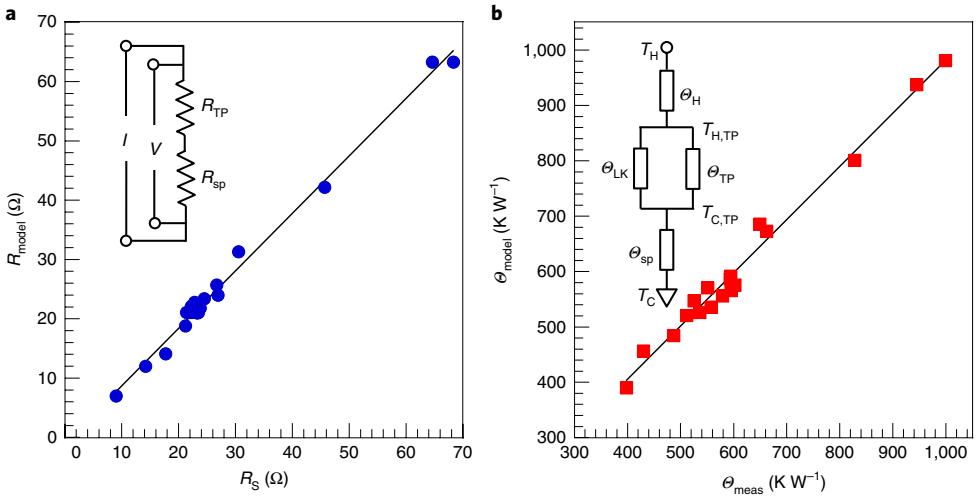

Fig. 3 | Electrical resistance and thermal impedance models. a, Modelled electrical resistance R_{model} versus measured source resistance R_S for 19 variations of TEG circuit types. The line is a least-squares linear fit with the resistivities of the material components as fitting parameters. Inset, schematic of the series resistor network consisting of the intrinsic thermopile resistance R_{TP} and a parasitic spreading resistance R_{sp}. **b**, Modelled thermal impedance Θ_{model} versus measured thermal impedance Θ_{meas} for 19 variations of TEG circuit types. The line is a least-squares linear fit with the thermal conductivities of the material components as fitting parameters. Inset, schematic of the series thermal impedance network from the heater at temperature T_H to thermal ground at temperature T_C.

circuit layout parameters determine R_{TP} and parasitic resistances. The ability to engineer R_S is crucial because, for the same V_{OC}, $P_{max} \propto 1/R_S$, so it appears one wants to minimize R_S. However, in real applications where a TEG powers a load resistance R_L, the goal is usually to maximize power to the load, which requires matched load conditions. Hence, given an R_L, the TEG should be engineered to make $R_S = R_L$, not to minimize R_S. It is desirable to have R_S dominated by R_{TP}, because parasitic resistances do not generate power but only dissipate it internally. From the model results, we find R_{TP}/R_S is between 0.90 and 0.93 across all TEG variations, so parasitic resistances account for ≤10% of R_S. This level of control and minimization of parasitic resistances, made possible in CMOS technology, enhances the power generation capacity.

Figure 3b presents a scatter plot of the modelled thermal impedance Θ_{model} versus Θ_{meas} across 19 different circuit variations along with the least-squares fit line. Each point represents a DUT of one circuit variant with its layout geometry and dimensions used to calculate Θ_{model}, but every point in Fig. 3b uses the same material thermal conductivity values determined from the least-squares fit. If Θ_{model} exactly described Θ_{meas}, the scatter plot would form a line with unity slope. Figure 3b shows that Θ_{model} is linearly related to Θ_{meas} with a slope of 0.962 and $r^2 = 0.985$. This indicates that the model provides a realistic physics-based representation of the thermal impedances among all these TEG circuit variants.

Thermal impedances between the heater and the thermopile top and between the chuck and the thermopile bottom cause the temperature at the thermopile top ($T_{H,TP}$) to be less than T_H and the temperature at the thermopile bottom ($T_{C,TP}$) to be greater than T_C. Thus $\Delta T_{TP} = T_{H,TP} - T_{C,TP} < \Delta T = T_H - T_C$. Using the thermal circuit from the inset of Fig. 3b and the thermal impedance values generated by the model allows us to estimate ΔT_{TP}. An ideal TEG with no parasitic thermal impedances would have $\Delta T_{TP}/\Delta T = 1$. In our devices, for $\Delta T = 20$ K the model gives ΔT_{TP} between 2.0 and 3.5 K, depending on the circuit variant type, with most types having ΔT_{TP} near 2.5 K. In particular, the DUT of Fig. 1 had $\Delta T_{TP} = 2.7$ K. The ratio $\Delta T_{TP}/\Delta T = 0.10$–$0.18$ in our devices is less than unity but is better than that reported in refs. [23–31], using both harvest and test modes, where $\Delta T_{TP}/\Delta T$ is typically between 0.005 and 0.10.

Analysis of IC TEG circuit performance

Using the impedance models, we can assess quantitatively the performance of our TEG devices and how improvements can be made in subsequent designs. Using $T_{H,TP}$, $T_{C,TP}$ and Q, we can compute the intrinsic net thermopower S_{TP} and efficiency η_{TP} of the thermopile de-embedded from the circuit. The intrinsic voltage, $S_{TP}\Delta T_{TP}$, generated by the thermopile itself through its intrinsic source resistance R_{TP} is related to the measured V_{OC} by a voltage divider equation $V_{OC} = (S_{TP}\Delta T_{TP})(R_{TP}/R_S)$. Using this for the DUT of Fig. 2, we find $S_{TP} \approx 1.1$ mV K^{-1}.

The intrinsic thermopile efficiency η_{TP} is best considered relative to the Carnot efficiency $\eta_{Carnot} = \Delta T_{TP}/T_{H,TP}$. The DUT used for Fig. 2 had the highest $\eta_{TP}/\eta_{Carnot} = 7 \times 10^{-4}$, comparable to the efficiencies reported for Si TEGs but much lower than that of high-ZT TEGs. Our ZT can be estimated either by using the ideal efficiency for a matched load $R_L = R_S$ (ref. [12])

$$\frac{\eta_{TP}}{\eta_{Carnot}} = \frac{2ZT}{4ZT + ZT\left(1 - \frac{T_{C,TP}}{T_{H,TP}}\right) + 4\left(1 + \frac{T_{C,TP}}{T_{H,TP}}\right)} \quad (1)$$

or by using the values of S_{TP} and the thermal conductivity and electrical resistivity extracted from the impedance models. Both methods yield an estimated $ZT \approx 3 \times 10^{-3}$ to 5×10^{-3}, indistinguishable from bulk Si at similar dopant densities.

A question of significant interest to device physics is whether the ZT of these nanoblades could be improved. We explored this issue through a set of four device variations with the same layout but different blade widths $w = 80$, 120, 160 and 240 nm. In particular, all four variants held constant the cumulative nanoblade cross-sectional areas $A_n = N_n wL$ for n-type and $A_p = N_p wL$ for p-type, where N_n and N_p are the number of n- and p-blades and $L = 750$ nm is the fixed blade length. N_n and N_p were adjusted to keep A_n and A_p constant as w varied. Figure 4 presents a graph of R_{TP} and P_{max} (at $\Delta T = 20$ K) versus w. As expected for a constant cumulative cross-section, R_{TP} is nearly independent of w, varying <4% about the mean. P_{max}, however, increases by almost 10× as w decreases from 240 to 80 nm, suggesting that the efficiency and ZT increase significantly with decreasing w around this length scale. This is consistent with the

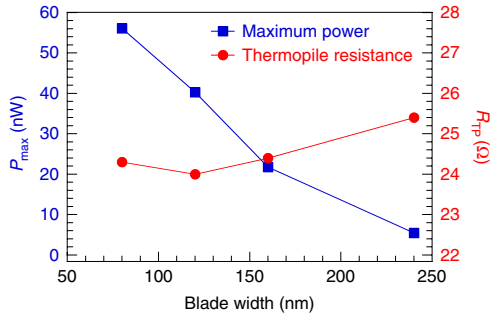

Fig. 4 | Maximum power dependence on nanoblade width. Measured maximum power (blue squares, left axis) at $\Delta T = 20$ K and thermopile resistance R_{TP} (red circles, right axis) plotted versus nanoblade width for four TEG circuit variations. These circuit variants had fixed cumulative nanoblade cross-sectional areas but different blade widths *w* adjusting the number of n- and p-blades, to keep the cumulative areas constant. The lines are guides to the eye that connect the data points.

argument that restricting the phonon mean free path by narrowing a physical dimension can increase *ZT*. This result strongly suggests that going to a nanowire geometry using 65 nm node technology, or going to a sub-65 nm node technology to fabricate narrower blades, will greatly improve performance.

There are two main reasons why the Γ_P values of our Si IC TEGs can be comparable to those of high-*ZT* TEGs despite having much lower efficiency. The first is that CMOS processing can fabricate a high number of thermocouples per unit area and still maintain a low areal packing fraction. Counting a pair of nanoblade groups as a thermocouple, the layout of Fig. 1c has a thermocouple number density of $>4\times10^6\,cm^{-2}$. Using CMOS processing, this density is scalable to macroscopic dimensions; fabricating $\geq1\,cm^2$ area thermopiles at this density would not add processing steps, time or cost. By comparison, (Bi,Sb,Pb)(Te,Se) TEGs have thermocouple densities of $\leq1\times10^4\,cm^2$. Thus the lower *ZT* of our Si nanoblades can be compensated by a higher number of thermocouples per unit area. However, simply making a thermopile with high thermocouple areal density is insufficient to yield a high Γ_P. As derived in ref. [34], given a series thermal impedance $\Theta_S > 0$ and leakage $\Theta_{LK} < \infty$, the thermopile's Θ_{TP} has an optimal value $\Theta_{TP,opt} = \Theta_S\Theta_{LK}/(\Theta_S + \Theta_{LK})$ that maximizes $\Delta T_{TP}/\Delta T$ and P_{max}. Because $\Theta_{TP} \propto$ (areal density of thermocouples)$^{-1}$, too high a thermocouple density can make $\Theta_{TP} < \Theta_{TP,opt}$ and thus degrade Γ_P by dragging down ΔT_{TP}. The key is to control Θ_{TP} by making a high thermocouple density but with relatively low packing fraction. This may be an issue with the Si nanowire TEG of ref. [23], which used a packing fraction of 60% and gave an estimated $\Delta T_{TP}/\Delta T \approx 0.02$ and $\Gamma_P = 0.0004\,\mu W\,cm^{-2}K^{-2}$. By contrast, all our devices had packing fractions of 2–3%, which contributed to a relatively high $\Delta T_{TP}/\Delta T$. To accomplish this required the ability of CMOS processing to fabricate a large number of very small-area structures with high uniformity.

The second reason for the relatively high Γ_P in our Si IC TEGs comes from the ability of CMOS to engineer electrical and thermal impedances with control unmatched by any other process technology. For example, increasing the number of thermocouples alone increases R_{TP} because the thermocouples are electrically connected in series, which may make it difficult to match to a specified R_L. However, because CMOS can control n- and p-dopant densities across many orders of magnitude (10^{16} to $10^{20}\,cm^{-3}$), increasing the number of series-connected resistor elements can be compensated to a large extent by adjusting the dopant densities to decrease the resistance per element. Thus, R_{TP} can still be made to match a given R_L across a wide range of R_L. In our devices, for TEGs of the same layout, R_{TP} could be made to range from $<5\,\Omega$ to $>200\,\Omega$ by changing the dopant density. In addition, use of a silicide grid greatly reduced the spreading resistance between the thermopile elements and the electrical leads. This resulted in the R_S being dominated by the thermopile R_{TP} rather than by parasitics.

Equally important is thermal impedance management. CMOS processing allowed us to experiment with different metallization layouts aimed at reducing the parasitic series thermal impedance from the T_H reservoir to the top of the thermopile, resulting in relatively high values of $\Delta T_{TP}/\Delta T$. There is no reason to think that the parasitic thermal impedance cannot be further reduced in future designs, perhaps by incorporating higher thermal conductivity CMOS-compatible dielectrics such as SiC in the thermal path from the hot reservoir to the thermopile. The ability to mix these Si TEGs among other circuitry on an IC chip also allows the possibility of distributing thermopile clusters across the chip so as to maximize the thermal coupling of the TEG to the main areas of on-chip heat generation (essentially test mode), each of which will have a different thermal source impedance. While this would require careful consideration of chip floor plan and package thermal characteristics, it ultimately represents a major advantage of an integrated TEG.

Conclusions

Using industrially standard 65 nm technology Si CMOS processing, we fabricated prototype Si IC TEGs using nanostructured Si blades as the thermopile elements. While the thermopile *ZT*, and thus the efficiency of these Si TEGs, lags behind more exotic high-*ZT* materials, the specific power generation capacity (Γ_P) of our Si IC TEGs is comparable to that of microelectronic TEGs using high-*ZT* materials. This is important because, in many applications, Γ_P is a more critical performance metric than efficiency. The high Γ_P is achieved because industrial CMOS techniques can fabricate a very high areal density of thermocouples, while keeping the packing fraction relatively low to optimize thermal and electrical circuit impedances. The empirical results and modelling establish directions for improving performance in future designs. In particular, these Si IC TEGs also show evidence that efficiency can be improved markedly by moving to smaller blade dimensions or nanowire geometries. Finally, because these TEGs were fabricated on an industrial process line respecting process design rules, they can be integrated on-chip with other Si CMOS electronic circuits in a commercially scalable manner with nearly zero marginal cost.

Methods

Device fabrication and dimensions. The Si IC TEGs used were all fabricated using industrially standard 65 nm node process technology beginning with a 300-mm-diameter p-type Si wafer on a commercial process line. The Si nanostructured blades used as thermopile elements were formed by the same photolithographic masking and moat etch process normally used to create isolation trenches for Si CMOS transistors in this process technology. The baseline blade dimensions were 80 nm width × 750 nm length × 350 nm height, with some circuit variants having greater widths. The n-type blades were etched from n^+-wells ($\sim1\times10^{18}\,cm^{-3}$) formed by P and As ion implantation, and p-type blades were etched from p^+-wells ($\sim1\times10^{18}\,cm^{-3}$) formed by B ion implantation. SiO_2 filled the space between blades for mechanical support. Blades of the same dopant polarity were grouped into sets of two to six to form one leg of a thermocouple. A baseline TEG device consisted of 48 n-type and 96 p-type blade groups occupying a total planar area of 48 μm × 36 μm.

Thermopile measurement protocol. The original 300-mm-diameter processed wafer was diced into 20 mm × 30 mm die. A die of TEG devices under test (DUTs) was placed on a gold-plated copper chuck in an enclosed probe station. A thin layer of thermal grease applied to the underside of the die greatly improved thermal contact to the chuck. A calibrated platinum resistor thermometer embedded in the chuck monitored the chuck temperature (used as T_C in TEG measurements), and two more calibrated thermometers monitored the environmental temperature in the probe station. On a given DUT, a four-contact Kelvin probe configuration was used to measure the thermopile current–voltage (*I*–*V*) behaviour, and four other probes controlled the current and voltage of the heater resistor (shown at the top of Fig. 1c). Thermopile *I*–*V* measurements were taken with an Agilent 4156C

semiconductor parameter analyser, while the heater resistor was controlled using a temperature controller. The first step in measuring any particular DUT was to calibrate the temperature dependence of its heater resistor, allowing the heater resistor to be used as both the high-temperature reservoir and thermometer to determine T_H. Details of this calibration procedure are given in the next section. After calibrating the heater resistor, the measurement protocol of the TE response of the DUT was as follows. First, the I–V data of the thermopile were measured from −0.5 to +0.5 V with no power to the heater, setting the equilibrium $\Delta T = 0$ characteristics. At $\Delta T = 0$ the thermopile I–V was linear in every DUT and crossed $V = I = 0$ within measurement uncertainty. Then, the heater was brought up to a target temperature T_H using its temperature controller, while monitoring T_C. After the heater stabilized at T_H for at least 2 min, the thermopile I–V measurements were taken at $\Delta T = (T_H - T_C)$. This procedure was repeated for several ΔT values between 5 and 70 K. On some DUTs, thermopile I–V measurements were remeasured at the same ΔT while decreasing the temperature from the maximum ΔT to check for possible thermal hysteresis. No significant thermal hysteresis was observed. For T_H as high as 365 K, T_C did not increase by more than 0.1 K from its room-temperature value. This is expected, because the thermal mass of the chuck is many orders of magnitude greater than that of the Si die, so the chuck acts an ideal cold reservoir.

Calibration of heater resistor temperature dependence. For each DUT, the resistance R_0 of the heater resistor at room temperature, $T_0 = 295 \pm 1$ K (depending on the day, as measured by the chuck and probe station thermometers), was determined using a Kelvin probe configuration at low bias ($V_{bias} = 0.01$ V) to avoid self-heating effects. R_0 for different DUTs varied in the range 70–150 Ω due to the different meander lengths of each DUT's heater line. The environmental temperature of the probe station was gradually increased and the heater resistance $R(T)$ was measured, again using $V_{bias} = 0.01$ V, where the power applied to the heater was <1.5 μW to avoid self-heating. For these $R(T)$ measurements, the linearity of the heater resistor's I–V characteristics between ±0.01 V bias was confirmed up to the highest temperature used (365 K). The linear temperature coefficient of resistance, $TCR = (1/R_0)[(R(T) - R_0)/(T - T_0)]$, was then determined. All DUTs had nearly the same $TCR = (2.7 \pm 0.2) \times 10^{-3}\,K^{-1}$, independent of the room-temperature value of the resistance, where the ±0.2 uncertainty encompasses the spread in TCR values among all DUTs measured. When used as a heater for TEG measurements, the heater resistor was voltage-biased to suppress positive thermal feedback at V_{bias} ranging from 0.5 to 3.0 V. The temperature T_H was determined from its linear (not differential) resistance $R(T_H) = V_{bias}/I_{bias} = R_0[1 + TCR(T_H - T_C)]$, where T_C was the temperature of the chuck.

Electrical and thermal impedance modelling. The source resistance R_S measured by a four-point Kelvin probe excludes all lead and contact resistances up to the silicide grid. However, in addition to the thermopile's intrinsic resistance R_{TP}, R_S includes a series internal parasitic resistance that calculations show is primarily due to the spreading resistances R_{sp} in the n^+- and p^+-wells from thermopile bottom to the silicide grid. A simple schematic of this series resistor network is drawn in the inset of Fig. 3a. We developed model expressions for R_{TP} and R_{sp} that incorporate the particular design of each TEG circuit type, such as nanoblade dimensions, number and spacing of nanoblades in a group and mean distance from nanoblade groups to the silicide grid. We then ran a numerical least-squares linear fit using Matlab of the set of modelled resistances $R_{model} = R_{TP} + R_{sp}$ for each circuit type to the set of measured R_S values. In R_{model}, for each circuit type the layout geometries and dimensions were fixed using design values, while the resistivities of the component materials were treated as fitting parameters. Common literature values of material resistivities were used as the initial guesses in the fitting routine. The thermal impedance model attempts to replicate all significant heat flow paths from the heater at temperature T_H to the chuck at temperature T_C, regarded as the thermal ground, as depicted in the inset of Fig. 3b. We developed a model expression for each Θ term in this circuit that accounts for the specific geometry and dimensions of each TEG circuit type. Θ_H represents the series thermal impedance from the heat source to the top of the thermopile and includes factors such as distance and overlap area between the heater and its box, as well as areas and thicknesses of dielectric fillers, metal lines, metal vias and W plugs. Θ_{TP} is the thermal impedance of the thermopile itself and accounts for the dimensions, number, size and grouping of the n- and p-nanoblades. Θ_{LK} is the parallel leakage thermal impedance accounting for heat flow through the dielectric filler surrounding and thus bypassing the nanoblades. Θ_{sp} is the thermal spreading impedance into the n^+- and p^+-wells and into the substrate and chuck. We then ran a least-squares linear fit using Matlab of the set of modelled thermal impedances Θ_{model} for all DUT types to the set of measured Θ_{meas}, using thermal conductivities of the component materials as fitting parameters. Literature values of thermal conductivities were used as the initial guesses in the fitting routine.

Data availability

The numerical data used to generate Figs. 2–4 in this Article are available from the corresponding author on reasonable request.

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Author contributions

G.H. made measurements, developed and wrote modelling code, and analysed data. H.E. designed the devices, supervised fabrication of the devices and analysed data. M.L. set up measurements, validated data and modelling, and analysed data.

Competing interests

The fabrication and design of all TEG devices used in this work was supported by Texas Instruments. H.E. is an employee of Texas Instruments.

Additional information

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